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				<b>First Named Inventor</b>	Tsern et al.
				<b>Art Unit</b>	3694
<b>Examiner Name</b>	Cheung, Mary Da Zhi Wang				
<b>Sheet</b>	1	of	1	<b>Attorney Docket Number</b>	60809-0146-US

U.S. PATENT DOCUMENTS							
Examiner Initials	Cite No.	Document Number Number - Kind Code <sup>1</sup>	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Filing Date if Appropriate

FOREIGN PATENT DOCUMENTS								
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		Country Code <sup>2</sup> - Number <sup>3</sup> - Kind Code <sup>4</sup> (if known)					Yes	No

OTHER NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		BURSKY, "Memory-CPU Interface Speeds Up Data Transfers," Electronic Design, pp. 137-142, March 19, 1992.
		CHOI, "16Mbit Synchronous DRAM with 125Mbyte/sec Data Rate," Symposium on VLSI Circuits, Digest of Technical Papers, pp. 65-66, 1993.
		GARY et al., "The PowerPC™ 603 Microprocessor: A Low-Power Design for Portable Applications," IEEE Design & Test of Computers, Winter, 1994.
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		LINES et al., "High Speed Circuit Techniques in a 150Hz 64M SDRAM," Proceedings of Memory Technology, Design & Testing Int'l Workshop, San Jose, California, August 11, 1997, pp. 8-11.
		SAEKI et al., "A 2.5ns Clock Access, 250MHz 256Mb SDRAM with Synchronous Mirror Delay," IEEE ISSCC Digest of Technical Papers, pp. 374-375, 476, 1996.

<b>Examiner Signature</b>		<b>Date Considered</b>	
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